Claims

What is claimed is:

1. A method for transferring data on a bus from a source to at least two destinations substantially simultaneously, comprising the steps of:

supplying data from the source to first of said at least two destinations as a read data operation; and

supplying data to a second of said at least two destinations as a write operation.

2. The method according to claim 1, wherein the source comprises a non-addressed data device.

3. The method according to claim 2, wherein the source comprises a FIFO device.

4. The method according to claim 1, wherein at least one of the at least two destinations comprise addressed data devices.

5. The method according to claim 4, wherein the at least one destinations comprises a microprocessor.

6. The method according to claim 4, wherein the at least one destinations comprises a memory storage.

7. The method according to claim 4, wherein the at least one destinations comprises a SDRAM memory.

8. An apparatus for transferring received data from a network, comprising:

a bus;

a media access controller for putting the received data from the network onto said bus;

a microprocessor for reading the data from said bus;

a memory for writing the data from said bus into said memory; and

a timing controller for controlling said media access controller, said microprocessor and said memory to have said media access controller write the data to the bus, said memory write the data to said memory and said microprocessor read the data substantially simultaneously.

9. An apparatus for transferring data, comprising:

a bus;

a FIFO data source connected to said bus for putting data onto said bus;

a microprocessor connected to said bus for reading the data from said bus;

a memory connected to said bus for writing the data from said bus into said memory; and

a timing controller connected to said FIFO data source, said microprocessor and said memory for controlling said FIFO data source, said microprocessor and said memory to have said FIFO data source put the data onto the bus, said memory write the data to said memory and said microprocessor read the data substantially simultaneously.

Add 31